**IEEE 123 Bus system in Simulink v2019b**

* Two models are created, one with lines modelled as Distributed parameters Line (DPL) and other with lines modeled as Pi Section Line(PI)
* Voltage regulators are modelled and includes LDC
* Initial Tap settings are taken same as the benchmark document
* Runs in Phasor domain. Simulation is much faster compared to the discrete domain simulation.

**Regulator taps and Parameters**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Regulator ID: | 1 |  |  |  | Regulator ID: | 3 |  |  |
| Line Segment: | 150 - 149 |  |  |  | Line Segment: | 25 - 26 |  |  |
| Phases: | A-B-C |  |  |  | Phases: | A-C |  |  |
| Connection: | 3-Ph, Wye |  |  |  | Connection: | 2-Ph,L-G |  |  |
| Monitoring Phase: | A |  |  |  | Monitoring Phase: | A & C |  |  |
| Bandwidth: | 2.0 volts |  |  |  | Bandwidth: | 1 |  |  |
| PT Ratio: | 20 |  |  |  | PT Ratio: | 20 |  |  |
| Primary CT Rating: | 700 |  |  |  | Primary CT Rating: | 50 |  |  |
| Compensator: | Ph-A |  |  |  | Compensator: | Ph-A | Ph-C |  |
| R - Setting: | 3 |  |  |  | R - Setting: | 0.4 | 0.4 |  |
| X - Setting: | 7.5 |  |  |  | X - Setting: | 0.4 | 0.4 |  |
| Voltage Level: | 120 |  |  |  | Voltage Level: | 120 | 120 |  |
| Time Delay Assumed(s): | 10 | 10 | 10 |  | Time Delay Assumed(s): | 20 | 20 |  |
|  |  |  |  |  |  |  |  |  |
| Regulator ID: | 2 |  |  |  | Regulator ID: | 4 |  |  |
| Line Segment: | 9 - 14 |  |  |  | Line Segment: | 160 - 67 |  |  |
| Phases: | A |  |  |  | Phases: | A-B-C |  |  |
| Connection: | 1-Ph, L-G |  |  |  | Connection: | 3-Ph, LG |  |  |
| Monitoring Phase: | A |  |  |  | Monitoring Phase: | A-B-C |  |  |
| Bandwidth: | 2.0 volts |  |  |  | Bandwidth: | 2 |  |  |
| PT Ratio: | 20 |  |  |  | PT Ratio: | 20 |  |  |
| Primary CT Rating: | 50 |  |  |  | Primary CT Rating: | 300 |  |  |
| Compensator: | Ph-A |  |  |  | Compensator: | Ph-A | Ph-B | Ph-C |
| R - Setting: | 0.4 |  |  |  | R - Setting: | 0.6 | 1.4 | 0.2 |
| X - Setting: | 0.4 |  |  |  | X - Setting: | 1.3 | 2.6 | 1.4 |
| Voltage Level: | 120 |  |  |  | Voltage Level: | 124 | 124 | 124 |
| Time Delay Assumed(s): | 20 |  |  |  | Time Delay Assumed(s): | 20 | 20 | 20 |

**Comparison of Steady state voltages and Substation Power**

|  |  |  |  |
| --- | --- | --- | --- |
| **Substation Active Power (KW)** | **Phase a** | **Phase b** | **Phase c** |
| Benchmark | 1463.861 | 963.484 | 1193.153 |
| Simulink DPL | 1492 | 999.2 | 1220 |
| Simulink PI | 1491 | 998 | 1225 |

|  |  |  |  |
| --- | --- | --- | --- |
| **Substation Reactive Power (KVar)** | **Phase a** | **Phase b** | **Phase c** |
| Benchmark | 582.101 | 343.687 | 398.976 |
| Simulink DPL | 595.1 | 364 | 415.1 |
| Simulink PI | 597 | 363.7 | 412.8 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Tap Setting** | **Regulator 1** | **Regulator 2** | **Regulator 3** | **Regulator 4** |
| Benchmark | 7 7 7 | -1 NA NA | 0 NA -1 | 8 1 5 |
| Simulink(Initial) | 7 7 7 | -1 NA NA | 0 NA -1 | 8 1 5 |
| Simulink(Final) | 7 7 7 | -1 NA NA | 1 NA -1 | 9 2 5 |

**Phase A Voltage**

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**Phase B Voltage**

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**Phase C Voltage**

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**% Difference in Voltage due to Assumptions and Approximations**

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|  |  |  |  |
| --- | --- | --- | --- |
| **Max Error pu** | **Phase a** | **Phase b** | **Phase c** |
| Simulink DPL | 0.0072 | 0.0138 | 0.0079 |
| Simulink DPL | 0.0094 | 0.0150 | 0.0078 |

The main reason for the difference in voltage compared to benchmark is due to the assumptions and approximations taken as given below

* Dynamic Simulation in Simulink will consider all Loads as Constant Impedance Loads